Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-25 (cancelled)

26. (new) A method for manufacturing a semiconductor integrated circuit device including a memory cell of an SRAM having a first p-channel MISFET and a first n-channel MISFET, and a peripheral circuit having a second p-channel MISFET and a second n-channel MISFET, comprising:

providing a silicon on insulator substrate including an insulated layer and a semiconductor layer formed on said insulated layer,

wherein said semiconductor layer has a memory cell forming region and a peripheral circuit forming region,

wherein said memory cell forming region includes a first p-channel MISFET forming region where said first p-channel MISFET is to be formed and a first n-channel MISFET forming region where said first n-channel MISFET is to be formed,

wherein said peripheral circuit forming region includes a second p-channel MISFET forming region where said second p-channel MISFET is to be formed and a second n-channel MISFET forming region where said second n-channel MISFET is to be formed;

selectively introducing a first impurity into said first p-channel MISFET forming region and said second p-channel MISFET forming region for controlling a threshold voltage;

selectively introducing a second impurity into said first n-channel MISFET forming region and said second n-channel MISFET forming region for controlling a threshold voltage;

selectively introducing a third impurity into said first p-channel MISFET forming region by using a mask covering said second p-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of said first p-channel MISFET is higher than a threshold voltage of said second p-channel MISFET; and

selectively introducing a fourth impurity into said first n-channel MISFET forming region by using a mask covering said second n-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of said first n-channel MISFET is higher than a threshold voltage of said second n-channel MISFET.

27. (new) A method for manufacturing a semiconductor integrated circuit device according to claim 26, further comprising:

forming a groove in said semiconductor layer for defining said first p-channel MISFET forming region, said first n-channel MISFET forming region, said second p-channel MISFET forming region and said second n-channel MISFET forming region; and

burying an insulating film in said groove by polishing an insulating film formed over said substrate having said groove.

28. (new) A method for manufacturing a semiconductor integrated circuit device according to claim 26, further comprising:

forming gate electrodes of said first n-channel MISFET, said first p-channel MISFET, said second n-channel MISFET and said second p-channel MISFET; and

forming a source and drain region of said first n-channel MISFET, said first p-channel MISFET, said second n-channel MISFET and said second p-channel MISFET.

29. (new) A method of manufacturing a semiconductor integrated circuit device, comprising:

providing a silicon on insulator substrate including an insulated layer and a semiconductor layer formed on said insulated layer,

wherein said semiconductor layer has a memory cell of SRAM having a first p-channel MISFET and a first n-channel MISFET, and a logic circuit for a microprocessor having a second p-channel MISFET and a second n-channel MISFET,

wherein said first p-channel MISFET is formed at a first p-channel MISFET forming region of said semiconductor layer,

wherein said first n-channel MISFET is formed at a first n-channel MISFET forming region of said semiconductor layer,

wherein said second p-channel MISFET is formed at a second p-channel MISFET forming region of said semiconductor layer,

wherein said second n-channel MISFET is formed at a second n-channel MISFET forming region of said semiconductor layer;

selectively introducing a first impurity into said first p-channel MISFET forming region and said second p-channel MISFET forming region for controlling a threshold voltage;

selectively introducing a second impurity into said first n-channel MISFET forming region and said second n-channel MISFET forming region for controlling a threshold voltage;

selectively introducing a third impurity into said first p-channel MISFET forming region by using a mask covering said second p-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of said first p-channel MISFET is higher than a threshold voltage of said second p-channel MISFET;

selectively introducing a fourth impurity into said first n-channel MISFET forming region by using a mask covering said second n-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of said first n-channel MISFET is higher than a threshold voltage of said second n-channel MISFET;

forming a groove in said semiconductor layer for defining said first p-channel MISFET forming region, said first n-channel MISFET forming region, said second p-channel MISFET forming region and said second n-channel MISFET forming region; and

burying said groove with an insulating film by polishing an insulating film formed over said semiconductor layer having said groove.

30. (new) A method of manufacturing a semiconductor integrated circuit device according to claim 29, wherein an operating speed thereof is 100 MHz or more.

31. (new) A method of manufacturing a semiconductor integrated circuit device, comprising:

providing a silicon on insulator substrate including an insulated layer and a semiconductor layer formed on said insulated layer,

wherein said semiconductor layer has a memory cell of an SRAM having a first p-channel MISFET and a first n-channel MISFET, and a peripheral circuit having a second p-channel MISFET and a second n-channel MISFET,

wherein said first p-channel MISFET is formed at a first p-channel MISFET forming region of said semiconductor layer,

wherein said first n-channel MISFET is formed at a first n-channel MISFET forming region of said semiconductor layer,

wherein said second p-channel MISFET is formed at a second p-channel MISFET forming region of said semiconductor layer,

wherein said second n-channel MISFET is formed at a second n-channel MISFET forming region of said semiconductor layer;

selectively introducing a first impurity into said first p-channel MISFET forming region and said second p-channel MISFET forming region for controlling a threshold voltage;

selectively introducing a second impurity into said first n-channel MISFET forming region and said second n-channel MISFET forming region for controlling a threshold voltage;

selectively introducing a third impurity into said first p-channel MISFET forming region by using a mask covering said second p-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of said first p-channel MISFET is higher than a threshold voltage of said second p-channel MISFET; and

selectively introducing a fourth impurity into said first n-channel MISFET forming region by using a mask covering said second n-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of said first n-channel MISFET is higher than a threshold voltage of said second n-channel MISFET;

forming a groove in said semiconductor layer for defining said first p-channel MISFET forming region, said first n-channel MISFET forming region, said second p-channel MISFET forming region and said second n-channel MISFET forming region; and

burying said groove with an insulating film by polishing an insulating film formed over said semiconductor layer having said groove.

32. (new) A method of manufacturing a semiconductor integrated circuit device according to claim 31, wherein an operating speed thereof is 100 MHz or more.

33. (new) A method of manufacturing a semiconductor integrated

circuit device including a memory cell of an SRAM having a first p-channel MISFET and a first n-channel MISFET, and a peripheral circuit having a second p-channel MISFET and a second n-channel MISFET, comprising:

(a) providing a semiconductor substrate having a memory cell forming region and a peripheral circuit forming region,

wherein said memory cell forming region includes a first p-channel MISFET forming region where said first p-channel MISFET is to be formed and a first n-channel MISFET forming region where said first n-channel MISFET is to be formed,

wherein said peripheral circuit forming region includes a second p-channel MISFET forming region where said second p-channel MISFET is to be formed and a second n-channel MISFET forming region where said second n-channel MISFET is to be formed;

(b) selectively introducing a first impurity into said first p-channel MISFET forming region and said second p-channel MISFET forming region for controlling a threshold voltage;

(c) selectively introducing a second impurity into said first n-channel MISFET forming region and said second n-channel MISFET forming region for controlling a threshold voltage;

(d) selectively introducing a third impurity into said first p-channel MISFET forming region by using a mask covering said peripheral circuit forming region for controlling a threshold voltage such that a threshold voltage of said first p-channel MISFET is higher than threshold voltages of said second p-channel MISFET and said further MISFET;

(e) introducing a fourth impurity into said first n-channel MISFET

forming region by using a mask covering said peripheral circuit forming region for controlling a threshold voltage such that a threshold voltage of said first n-channel MISFET is higher than threshold voltages of said second n-channel MISFET and said further MISFET;

(f) forming a mask pattern for exposing a first region where a MISFET having a relatively higher operating speed is to be formed in said peripheral circuit,

wherein said mask pattern covers said memory cell forming region and a second region in said peripheral circuit forming region where a MISFET is to be formed; and

(g) introducing a fifth impurity into said first region of said peripheral circuit forming region by using said mask pattern as a mask for controlling a threshold voltage such that a threshold voltage of said MISFET to be formed in said first region is lower than a threshold voltage of said MISFET to be formed in said second region.

34. (new) A method of manufacturing a semiconductor integrated circuit device according to claim 33, including forming gate insulating films for said MISFET to be formed in said first region and said MISFET to be formed in said second region wherein a thickness of a gate insulating film of said MISFET formed in said first region is thinner than a gate insulating film of said MISFET formed in said second region.

35. (new) A method of manufacturing a semiconductor integrated circuit device according to claim 33, further comprising:

forming a groove in said substrate for defining said first p-channel MISFET forming region, said first n-channel MISFET forming region, said second p-channel MISFET forming region, said second n-channel MISFET forming region and said further MISFET forming region; and

burying an insulating film in said groove by polishing an insulating film formed over said substrate having said groove.